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L#	Hits	Search String	Databases
S1	566094	(integrated or digital) near2 circuit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	40	S1 and ((bus near2 (performance or traffic)) with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	1665	S1 and (bus with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	2232	S1 and (bus near2 (performance or traffic))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	210	S3 and S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	210	S2 or S5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	23	S6 and (high near2 level near2 language$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	173	S6 and (source$1 or algorithm)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	88	S6 and (source$1 and algorithm)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	27	S6 and (bus with hardware with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	156	S6 and (bus with data with transfer$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	8	S6 and (evaluation with function$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	11	S6 and (modif$3 with source$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	1	S6 and ("general purpose" near2 language$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	60	S6 and (architecture with design)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	55	S11 and S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	24	S6 and (bus with process$3 with rate$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	2	S6 and (bus with traffic$3 with rate$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	132	S6 and (bus with traffic$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	11	S6 and (high near2 level near2 design$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	1	S6 and (performance with (feed$3 near2 back))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	1	S6 and ((evaluation or verification) with (feed$3 near2 back))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	24	S6 and (feed$3 near2 back)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	1	S6 and (syntax with (correction or analysis))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	103	S7 or S9 or S10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	72	S12 or S13 or S16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	7	S17 and S19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	51	S17 or S20 or S23 or S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	3687	S3 or S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	10	S30 and (syntax with (correction or analysis))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	138	S25 or S26 or S28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	566094	(integrated or digital) near2 circuit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	40	S32 and ((bus near2 (performance or traffic)) with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	1665	S32 and (bus with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	2232	S32 and (bus near2 (performance or traffic))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	210	S34 and S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S37	210	S33 or S36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S38	8	S37 and (evaluation with function$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S39	10	S37 and (bus with "data transfer" with evaluation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S40	11	S37 and (high near2 level near2 design$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S41	11	S37 and (modif$3 with source$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	24	S37 and (bus with process$3 with rate$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	5	S37 and (bus with processing with rate$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	3687	S34 or S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	7	S44 and (bus with "processing rate")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	3	S44 and (("high level" near2 design$1) with performance)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	55	S44 and ("high level" near2 design$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	24	S37 and (feed$3 near2 back)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	70	S44 and ((bus near2 performance) with (feedback$3 or (feed near2 back)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S50	943	S32 and (bus with simulat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	703	S50 and (source$1 or (programming near2 language$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	168	S51 and (bus with (performance or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	83	S52 and (hardware with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	403	S50 and (language$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	62	S53 and S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	1	S50 and ("bus traffic" with (count$3 or increment$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	1	S50 and (bus with traffic with (count$3 or increment$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	1	S50 and (bus with evaluation with increment$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

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Results of search set L29:S25 or S26 or S28

DocumentKind Codes	Title	Issue Date	Current OR	Abstract
US 20040123118 A1	Secure mode indicator for smart phone or PDA	20040624	713/189	
US 20040110519 A1	Source synchronous CDMA bus interface	20040610	455/502	
US 20040098701 A1	Automated repartitioning of hardware and software components in an embedded system	20040520	716/18	
US 20040090962 A1	Method and bit stream decoding unit for bit stream decoding	20040513	370/392	
US 20040081193 A1	Method for transmitting data within a communication system	20040429	370/458	
US 20040081079 A1	Method for monitoring a communication media access schedule of a communication control	20040429	370/216	
US 20040039865 A1	Efficient use of multiple buses for a scalable and reliable high-bandwidth connection	20040226	710/305	
US 20040006584 A1	Array of parallel programmable processing engines and deterministic method of operating th	20040108	718/107	
US 20030200425 A1	Devices, systems and methods for mode driven stops	20031023	712/229	
US 20030196144 A1	Processor condition sensing circuits, systems and methods	20031016	714/34	
US 20030172205 A1	Methods and components for mechanical computer	20030911	710/45	
US 20030163613 A1	DEBUG mode for a data bus	20030828	710/15	
US 20030144828 A1	Hub array system and method	20030731	703/21	
US 20030140245 A1	Secure mode for processors supporting MMU and interrupts	20030724	713/200	
US 20030140244 A1	Secure mode for processors supporting MMU	20030724	713/200	
US 20030140205 A1	Secure mode for processors supporting interrupts	20030724	711/163	
US 20030115564 A1	Block based design methodology	20030619	716/8	
US 20030115422 A1	System and method for managing data in an I/O cache	20030619	711/137	
US 20030101298 A1	Bus system and bus interface	20030529	710/107	
US 20030043790 A1	Multi-master bus architecture for system -on-chip designs	20030306	370/362	
US 20030014201 A1	FLOOR PLAN DEVELOPMENT ELECTROMIGRATION AND VOLTAGE DROP ANALYSIS T	20030116	702/64	
US 20020188892 A1	Method and apparatus for online detection and correction of faults affecting system-on-chip I	20021212	714/42	
US 20020183956 A1	Testing compliance of a device with a bus protocol	20021205	702/120	
US 20020166098 A1	Block based design methodology	20021107	716/1	
US 20020161907 A1	Adaptive multi-protocol communications system	20021031	709/230	
US 20020157042 A1	Algorithmically programmable memory tester with breakpoint trigger, error jamming and 'sco	20021024	714/45	
US 20020152060 A1	Inter-chip communication system	20021017	703/17	
US 20020129181 A1	High-performance communication architecture for circuit designs	20020912	710/113	
US 20020073380 A1	Block based design methodology with programmable components	20020613	716/1	
US 20020066082 A1	Bus performance evaluation method for algorithm description	20020530	717/135	
US 20020065972 A1	Bus system for use with information processing apparatus	20020530	710/305	
US 20020049879 A1	Cable and connection with integrated DVI and IEEE 1394 capabilities	20020425	710/305	
US 20020016952 A1	Block based design methodology	20020207	716/18	
US 20020013918 A1	Devices, systems and methods for mode driven stops	20020131	714/30	
US 20010042237 A1	Block based design methodology	20011115	716/8	
US 20010042147 A1	System-resource router	20011115	710/100	
US 20010039641 A1	Block based design methodology	20011108	716/8	
US 20010025369 A1	Block based design methodology	20010927	716/18	

US 20010018756 A1	Block based design methodology	20010830	716/1
US 20010016933 A1	Block based design methodology	20010823	716/1
US 6772295 B2	System and method for managing data in an I/O cache	20040803	711/137
US 6769046 B2	System-resource router	20040727	710/316
US 6760866 B2	Process of operating a processor with domains and clocks	20040706	714/34
US 6754763 B2	Multi-board connection system for use in electronic design automation	20040622	710/317
US 6725432 B2	Blocked based design methodology	20040420	716/4
US 6725306 B2	DEBUG mode for a data bus	20040420	710/107
US 6704895 B1	Integrated circuit with emulation register in JTAG JAP	20040309	714/726
US 6701504 B2	Block based design methodology	20040302	716/10
US 6698002 B2	Blocked based design methodology	20040224	716/4
US 6694501 B2	Block based design methodology	20040217	716/10
US 6681174 B1	Method and system for optimum bus resource allocation	20040120	701/117
US 6675139 B1	Floor plan-based power bus analysis and design tool for integrated circuits	20040106	703/17
US 6674750 B1	Apparatus and method for communicating time-division multiplexed data and packet data or	20040106	370/354
US 6658578 B1	Microprocessors	20031202	713/324
US 6651225 B1	Dynamic evaluation logic system and method	20031118	716/4
US 6631470 B2	Block based design methodology	20031007	716/3
US 6629293 B2	Block based design methodology	20030930	716/4
US 6622214 B1	System and method for maintaining memory coherency in a computer system having multipl	20030916	711/141
US 6622194 B1	Efficient use of multiple buses for a scalable and reliable high-bandwidth connection	20030916	710/305
US 6611739 B1	System and method for remote bus diagnosis and control	20030826	701/29
US 6594800 B2	Block based design methodology	20030715	716/1
US 6574778 B2	Block based design methodology	20030603	716/1
US 6567957 B1	Block based design methodology	20030520	716/4
US 6556899 B1	Bus diagnostic and control system and method	20030429	701/29
US 6546505 B1	Processor condition sensing circuits, systems and methods	20030408	714/30
US 6542968 B1	System and method for managing data in an I/O cache	20030401	711/137
US 6539497 B2	IC with selectively applied functional and test clocks	20030325	714/30
US 6522985 B1	Emulation devices, systems and methods utilizing state machines	20030218	702/117
US 6499123 B1	Method and apparatus for debugging an integrated circuit	20021224	714/724
US 6467009 B1	Configurable processor system unit	20021015	710/305
US 6463499 B1	Data bus cable having SCSI and IIC bus functionality and process for using the same	20021008	710/315
US 6457152 B1	Device and method for testing a device through resolution of data into atomic operations	20020924	714/738
US 6421251 B1	Array board interconnect system and method	20020716	361/788
US 6389379 B1	Converification system and method	20020514	703/14
US 6349392 B1	Devices, systems and methods for mode driven stops	20020219	714/30
US 6334164 B1	Bus system for use with information processing apparatus	20011225	710/316
US 6321366 B1	Timing-insensitive glitch-free logic system and method	20011120	716/6
US 6311296 B1	Bus management card for use in a system for bus monitoring	20011030	714/56
US 6269467 B1	Block based design methodology	20010731	716/1
US 6202103 B1	Bus data analyzer including a modular bus interface	20010313	710/15
US 6195744 B1	Unified multi-function operation scheduler for out-of-order execution in a superscaler proces	20010227	712/215
US 6195719 B1	Bus system for use with information processing apparatus	20010227	710/311
US 6173243 B1	Memory incoherent verification methodology	20010109	703/14
US 6154801 A	Verification strategy using external behavior modeling	20001128	710/119
US 6134516 A	Simulation server system and method	20001017	703/27
US 6123735 A	Method for simulating bus traffic	20000926	703/21
US 6098136 A	Multiple bus system using a data transfer unit	20000801	710/306
US 6085336 A	Data processing devices, systems and methods with mode driven stops	20000704	714/30
US 6081864 A	Dynamic configuration of a device under test	20000627	710/100
US 6073194 A	Transaction based windowing methodology for pre-silicon verification	20000606	710/100
US 6049847 A	System and method for maintaining memory coherency in a computer system having multipl	20000411	710/309
US 6032268 A	Processor condition sensing circuits, systems and methods	20000229	714/30
US 6026230 A	Memory simulation system and method	20000215	703/13

US 6009256 A	Simulation/emulation system and method	19991228	703/13
US 6006302 A	Multiple bus system using a data transfer unit	19991221	710/306
US 5935231 A	Bus system for use with information processing apparatus	19990810	710/306
US 5933158 A	Use of a link bit to fetch entries of a graphic address remapping table	19990803	345/568
US 5914730 A	System and method for invalidating and updating individual GART table entries for accelerat	19990622	345/531
US 5905509 A	Accelerated Graphics Port two level Gart cache having distributed first level caches	19990518	345/520
US 5897656 A	System and method for maintaining memory coherency in a computer system having multipl	19990427	711/141
US 5894575 A	Method and system for initial state determination for instruction trace reconstruction	19990413	717/128
US 5889971 A	Bus system for use with information processing apparatus	19990330	710/306
US 5884062 A	Microprocessor with pipeline status integrity logic for handling multiple stage writeback exce	19990316	712/218
US 5884059 A	Unified multi-function operation scheduler for out-of-order execution in a superscalar proces	19990316	712/215
US 5881261 A	Processing system that rapidly indentifies first or second operations of selected types for exe	19990309	712/214
US 5841670 A	Emulation devices, systems and methods with distributed control of clock domains	19981124	703/23
US 5826107 A	Method and apparatus for implementing a DMA timeout counter feature	19981020	710/27
US 5805792 A	Emulation devices, systems, and methods	19980908	714/28
US 5799165 A	Out-of-order processing that removes an issued operation from an execution pipeline upon c	19980825	712/214
US 5751976 A	Bus system for use with information processing apparatus	19980512	710/306
US 5745724 A	Scan chain for rapidly identifying first or second objects of selected types in a sequential list	19980428	712/213
US 5715433 A	Dynamic software model for emulating hardware	19980203	703/21
US 5668956 A	Bus system for use with information processing apparatus	19970916	710/306
US 5655145 A	Peripheral interface circuit which snoops commands to determine when to perform DMA pro	19970805	710/1
US 5630171 A	Translating from a PIO protocol to DMA protocol with a peripheral interface circuit	19970513	710/23
US 5621651 A	Emulation devices, systems and methods with distributed control of test interfaces in clock d	19970415	703/23
US 5603052 A	Interface circuit for transferring data between host and mass storage by assigning address ir	19970211	710/4
US 5600652 A	Local area network operating in the asynchronous transfer mode (ATM)	19970204	370/396
US 5592682 A	Interface circuit for transferring data between host device and mass storage device in respor	19970107	710/3
US 5584040 A	High performance peripheral interface with read-ahead capability	19961210	710/7
US 5535331 A	Processor condition sensing circuits, systems and methods	19960709	714/45
US 5506973 A	Bus system for use with information processing apparatus	19960409	710/305
US 5483642 A	Bus system for use with information processing apparatus	19960109	710/306
US 5384906 A	Method and apparatus for synchronizing a plurality of processors	19950124	709/400
US 5329471 A	Emulation devices, systems and methods utilizing state machines	19940712	703/23
US 5181201 A	Interface chip device	19930119	370/359
US 5179689 A	Dataprocessing device with instruction cache	19930112	710/22
US 5099417 A	Data processing device with improved direct memory access	19920324	710/27
US 4811237 A	Structured design method for generating a mesh power bus structure in high density layout c	19890307	716/9
US 4669079 A	Method and apparatus for bus arbitration in a data processing system	19870526	370/439
US 4658250 A	Computer network operating method and apparatus for detecting and exploiting data collisio	19870414	340/825.5
US 4591976 A	Multiple task oriented processor	19860527	714/20
US 4445172 A	Data steering logic for the output of a cache memory having an odd/even bank structure	19840424	711/3
US 4424561 A	Odd/even bank structure for a cache memory	19840103	711/3
US 4409656 A	Serial data bus communication system	19831011	709/250
US 4392201 A	Diagnostic subsystem for a cache memory	19830705	711/3
US 4378591 A	Memory management unit for developing multiple physical addresses in parallel for use in a	19830329	711/3
US 4363095 A	Hit/miss logic for a cache memory	19821207	711/206